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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. P043D2C2	SERIAL NUMBER 09/196,199
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE NOVEMBER 20, 1998	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
~~—~~	~~4,445,204~~	~~04/24/84~~	~~Nishiguchi~~			
TNT	4,821,226	04/11/89	Christopher et al.	364	926.1	
	4,882,712	11/21/89	Ohno et. al.	365	206	
	4,951,251	08/21/90	Yamaguchi et al.	365	189.02	
	4,928,265	12/29/92	Beighe et al.	365	189.01	
	5,107,465	04/21/92	Fung et al.	365	230.08	
—	~~5~~,206,833	04/27/93	Lee	365	~~233~~	
TNT	4,953,128	08/28/90	Kawai et al.	365	140	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
—	~~L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18~~ No. 5, ~~pp. 562-567 (Oct. 1983)~~
TNT	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
TNT	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
TNT	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)

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	~~4,206,833~~	~~04/27/93~~	~~Lee~~			
	~~4,953,128~~	~~08/28/90~~	~~Kawai et al.~~			
TNT	4,727,475	02/23/88	Kiremidjian	710	104	
	4,825,416	04/25/89	Tam et al.	365	194	
	4,891,791	01/02/90	Iijima	365	189.01	
TNT	5,140,688	08/18/92	White et al.	395	550	

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TNT	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
	~~F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA, 15-17 Sept. 1987~~
TNT	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
TNT	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)

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TNT	5,153,856	10/06/92	Takahashi	365	233	
	5,210,715	11/05/93	Houston	365	194	
	4,740,923	04/26/88	Kaneko et al.	365	194	
	4,953,130	08/28/90	Houston	365	203	
	4,792,926	12/20/88	Roberts	365	189.02	
	5,040,153	08/13/91	Fung et al.	365	230.03	
TNT	4,360,870	11/23/82	McVey	710	9	

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	~~F. Towler et. al., "A 128k 6.5ns Access/5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)~~
TNT	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference

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